CUSTOMER NO. 46900 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re: Attorney Docket No. Chen 3-1

In re application of: Jiashu Chen and Christopher A. Wendt

Serial No.:	09/190,208	Group Art Unit:	2643
Filed:	11/13/98	Examiner:	Lun-See Lao
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For: Method and Apparatus for Processing Interaural Time Delay in 3D Digital Audio

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reason(s) stated in the following Remarks/Arguments section.

REMARKS/ARGUMENTS

Previously presented claim 15 is directed to an apparatus for generating a delayed output digital audio signal from an input digital audio signal. The apparatus comprises first and second delay modules. The first delay module applies a first amount of delay to the input digital audio signal to generate a partially delayed digital audio signal, and the second delay module applies a second amount of delay to the partially delayed digital audio signal to generate the delayed output digital audio signal. The first delay module selects the first amount of delay from a plurality of available first delay values separated from one another by increments at a first resolution level, while the second delay module selects the second amount of delay from a plurality of available second delay values separated from one another by increments at a second resolution level different from the first resolution level.

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Certification Under 37 CFR 1.8

Date of Deposit 5/17/06

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail under 37 CFR 1.8 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

GERRY MARRERO
(Name of person mailing)

(Signature of person mailing)

Fig. 1 shows an exemplary embodiment of the apparatus of claim 15, where:

- Integer delay module **250** is an example of the first delay module of claim 15;
- Fractional delay module **252** is an example of the second delay module of claim 15;
- The signal from sound source **220** is an example of the input digital audio signal of claim 15;
- The signal transmitted from integer delay module **250** to fractional delay module **252** is an example of the partially delayed digital audio signal of claim 15; and
- Signal **262** is an example of the delayed output digital audio signal of claim 15.

According to the exemplary implementation described in the specification in the context of Fig. 2, the resolution level of integer delay module **250** is approximately 45 microseconds (uS) (see page 6, line 28), while the resolution level of fractional delay module **252** is about 0.7 uS (see page 7, line 13). In particular, integer delay module **250** can provide any delay value in the set {45 uS, 90 uS, 135 uS, ... }, up to some maximum delay value that depends on the size of the buffer used to implement integer delay module **250** (see page 6, lines 16-18), while fractional delay module **252** can provide any delay value in the set {0.7 uS, 1.4 uS, 2.1 uS, ..., 44.3 uS} (see page 7, lines 25-29).

Thus, in the exemplary embodiment of Fig. 2:

- Integer delay module **250** selects the first amount of delay from a plurality of available first delay values (i.e., {45 uS, 90 uS, 135 uS, ...}) separated from one another by increments at a first resolution level (i.e., 45 uS);
- Fractional delay module **252** selects the second amount of delay from a plurality of available second delay values (i.e., {0.7 uS, 1.4 uS, 2.1 uS, ..., 44.3 uS}) separated from one another by increments at a second resolution level (i.e., 0.7 uS); and
- The second resolution level (i.e., 0.7 uS) is different from the first resolution level (i.e., 45 uS).

In the final office action dated 3/10/06, the Examiner rejected independent claims 15, 33, and 49 under 35 U.S.C. 102(e) as being anticipated by Nagata (U.S. patent no. 5,974,154). In paragraph 3 of the final office action, the Examiner indicated that (1) Nagata's delay unit **61** is an example of the first delay module of claim 15 and (2) Nagata's delay unit **71** is an example of the second delay module of claim 15. According to the Examiner, (1) Nagata's delay values (GD1-GDn) provide an example of the plurality of available first delay values of claim 15 and (2) Nagata's delay values (GR1-GRn) provide an example of the plurality of available second delay values of claim 15.

Referring to Nagata's delay values (GD1-GDn) being separated from one another by increments at a first resolution level, the Examiner stated parenthetically at the bottom of page 2: "it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 by microcomputer 65 and see col. 4 line 60-col.5 line 67." Similarly, referring to Nagata's delay values (GR1-GRn) being separated from one another by increments at a second resolution level different from the first resolution level, the Examiner stated parenthetically on page 3: "it has a chance by adjusting the

state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 by microcomputer 65 and see col. 6 line 7-col.7 line 27."

Although the Examiner's language is confusing, the Applicant assumes that the Examiner believes that Nagata teaches that the resolution level of delay unit **61** can be different from the resolution level of delay unit **71**. The Applicant submits that (1) Nagata provides no such teaching and (2) the Examiner mischaracterized the teachings of Nagata.

There is strong evidence to suggest that the Examiner does not understand the difference between the concept of "an amount of delay" and the concept of "the increments between available amounts of delay." On page 12 of the final office action, the Examiner stated that "applicant argued in substance that in Nagata delay unit 61 and delay unit 71 do not produce different delays." The Applicant has never made any such argument. Rather, the Applicant has argued that, in Nagata, delay unit 61 and delay unit 71 have the same delay increments.

In any case, no matter what the Examiner believes or doesn't believe, the fact remains that Nagata provides no teaching or even suggestion that the resolution level of the increments between available delay values of delay unit 61 is different from the resolution level of the increments between available delay values of delay unit 71. Rather, all of the teachings in Nagata imply that the resolution levels of delay units 61 and 71 are identical.

As shown in Nagata's Fig. 2 and as taught in the corresponding portions of the specification, Nagata's delay units 61 and 71 are both memory units (e.g., RAMs) that receive a new data sample at every cycle of a sampling clock and provide delayed data samples at selected output ports (i.e., TD1, TD2, ..., TDn for delay unit 61, and TL1, TL2, ... TLn and TR1, TR2, and TRn for delay unit 71). See col. 4, lines 53-59, and col. 5, lines 14-21.

In the circuitry shown in Nagata's Fig. 2, data is input to and output from delay units 61 and 71 at the same rate (i.e., the sampling clock rate). In particular, at every sampling clock cycle:

- A new data sample from terminal 20 is applied to both adders 14 and 15;
- The output of adder 14 is applied to delay unit 61;
- At least one output of delay unit 61 (i.e., from at least one of output terminals TD1, TD2, ..., TDn) is applied to adder 63;
- The output of adder 63 is applied to adder 15;
- The output of adder 15 is applied to delay unit 71;
- At least one output of delay unit 71 (i.e., from at least one of output terminals TL1, TL2, ..., TLn) is applied to adder 72L; and
- At least one output of delay unit 71 (i.e., from at least one of output terminals TR1, TR2, ..., TRn) is applied to adder 72R.

The increments separating the available delay values for delay unit 61 are the differences between the delays associated with adjacent output terminals TD1, TD2, ..., TDn, such as the difference between the delay associated with output terminal TD2 and the delay associated with output terminal TD1. Similarly, the increments separating the available delay values for delay unit 71 are (1) the differences between the delays associated with adjacent output terminals TL1, TL2, ..., TLn, such as the difference between the delay associated with output terminal TL2 and the delay associated with output terminal TL1 and (2) the differences between the delays associated with adjacent output terminals TR1, TR2, ..., TRn, such as the difference between the delay associated with output terminal TR2 and the delay associated with output terminal TR1.

According to Nagata, output terminals TD1-TDn of delay unit 61 "output stepwise delayed signals having stepwise different delay times." See col. 4, lines 60-62. Similarly, "delay unit 71 outputs from terminals TL1-TLn and TR1-TRn delayed signals having stepwise different delayed times. See col. 5, lines 24-26.

According to Nagata, the range of delay times (i.e., the plurality of available delay values) can be changed using switch 50, while the particular delay time is selected using switch 48. See col. 7, lines 8-21. As shown in Fig. 4, the old range of stepwise different delay times starts at 100 msec and ends at 200 msec, while the new range of stepwise different delay times starts at 115 msec and ends at 215 msec. Significantly, however, for both ranges, the increments between the different delay times are identical (i.e., 5 msec). Thus, even though switches are adjusted, the resolution level of the different delay times remains unchanged.

On 5/3/06, the Applicant's below-named attorney Steve Mendelsohn had a telephonic interview with the Examiner in an attempt to explain to the Examiner the differences between the present invention and the teachings of Nagata. The Applicant thanks the Examiner for the courtesy of that interview.

During that interview, the Examiner argued that dials 41, 48, and 49 can be used to control the operations of delay units 61 and 71 such that their resolution levels will be different. The Applicant submits that there is no teaching in Nagata to support such a conclusion.

According to Nagata, dial 41 adjusts the echo level, which controls the gain factors or coefficients GD1-GDn and GF. See col. 6, lines 14-18. As such, this dial controls the strength (i.e., loudness) of the echo; it has nothing to do with the resolution level of available delay times.

Dial 48 is used to adjust the delay time (i.e., to select a different one of the available delay times), while dial 49 is used to adjust the repeat (i.e., the reverberation time). See col. 3, lines 51-52, and col. 6, lines 34-35. Significantly, according to Nagata, dial 48 of Fig. 3 has a pitch of 0.5. See col. 6, lines 64-66. In other words, dial 48 can assume any value from 0 to 10 in fixed 0.5 increments, as reflected in Fig. 4. These dials control the duration of the echo, but they do not change the resolution level of the available delay times.

In view of the foregoing, the Applicant submits that all of the teachings in Nagata support the conclusion that the resolution level of the increments separating the available delay values of delay unit 61 is identical to the resolution level of the increments separating the available delay values of delay unit 71. As such, the teachings of Nagata do not anticipate the subject matter of claim 15 and the rejection of claim 15 under 35 U.S.C. 102(e) is improper. The same applies to independent claims 33 and 49.

Respectfully submitted,

Steve Mendelsohn

Date: 5/17/06

Customer No. 46900
Mendelsohn & Associates, P.C.
1500 John F. Kennedy Blvd., Suite 405
Philadelphia, Pennsylvania 19102

Steve Mendelsohn
Registration No. 35,951
Attorney for Applicant
(215) 557-6657 (phone)
(215) 557-8477 (fax)